Low Temperature Wafer Bonding and Fine Pitch 3D Interconnect

Enabling a wide range of high performance, scalable, cost effective IC solutions with ZiBond® & DBI® technologies

Room Temp Bonding
Scalable to <1µm Pitch
Up to 15x Higher Throughput

Wafer-to-Wafer

**Image Sensor**
- De-facto industry standard technology for backside illuminated (BSI) image sensor
- Very fine pitch 3D interconnect, scalable to pixel-level
- Eliminates need for Thru Silicon Vias (TSVs)

**3D NAND**
- Memory array and logic disaggregation - enables technology node optimization
- Yield enhancement
- High speed memory I/O interfaces

Die-to-Wafer

**DRAM**
- Faster, cooler, smaller
- Very fine pitch 3D interconnect
- Eliminates under bump interconnect, microbumps, solder, and underfill

**RF**
- Reliably bonds dissimilar materials
- Improves thermal stability
- Enables RF CMOS transfer to a low cost, low RF loss substrate

MEMS
- Multi-function 3D integration
- Reliable hermetic seal
- Smaller footprint – eliminates pad limited die shrink

**2.5D/3D Logic**
- Increased memory to logic I/O and bandwidth
- Improves thermal performance
- Eliminates under bump interconnect, microbumps, solder, and underfill
### ZiBond® Technology

ZiBond technology is a low temperature homogeneous direct bonding solution that forms a strong bond between wafers or die with the same or different coefficients of thermal expansion (CTE). ZiBond technology is in high volume production today.

<table>
<thead>
<tr>
<th>Features</th>
<th>Bond Interface Materials</th>
<th>Substrates</th>
<th>Bonding Temperature</th>
<th>Anneal Temperature</th>
<th>Equipment</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SiO (TEOS, Thermal, Silane)</td>
<td>Si, Glass, InP, GaAs, GaN, SiC, LiTaO3, LiNbO3, Sapphire</td>
<td>Room Temperature</td>
<td>75-300°C (application dependent)</td>
<td>Industry standard wafer alignment and bonding equipment</td>
</tr>
</tbody>
</table>

### DBI® Technology

Direct Bond Interconnect (DBI) technology is a low temperature hybrid direct bonding solution that allows wafers or die to be bonded with exceptionally fine pitch 3D electrical interconnect. DBI can also minimize the need for Thru Silicon Vias (TSVs). DBI technology is in high volume production today.

<table>
<thead>
<tr>
<th>Features</th>
<th>3D Interconnect Pitch</th>
<th>Bond Interface Materials</th>
<th>Substrates</th>
<th>Bonding Temperature</th>
<th>Anneal Temperature</th>
<th>Equipment</th>
</tr>
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<tr>
<td></td>
<td>Scalable to &lt;1µm pitch 1.6µm demonstrated 6µm in high volume production</td>
<td>Same dielectrics as ZiBond with integrated metal interconnect</td>
<td>Same as ZiBond</td>
<td>Room Temperature</td>
<td>150-300°C (application dependent)</td>
<td>Industry standard wafer alignment and bonding equipment</td>
</tr>
</tbody>
</table>